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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,022	08/21/2006	Shunpei Yamazaki	0756-7803	6717

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	PAPER NUMBER
2812	
MAIL DATE	DELIVERY MODE
07/20/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/590,022	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-14,18,19 and 21* is/are rejected.

7)☒ Claim(s) *15-17,20,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/21/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed on 3/30/2009.

Currently, claims 11-23 are pending.

Election/Restrictions

1. Claims 1-10 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 3/30/2009.

2. Applicant's election without traverse of claims 11-23 in the reply filed on 3/30/2009 is acknowledged.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 11, 13, 18-19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (U.S. Publication No. 2003/0062845 dated 4/3/2003).

Yamazaki shows the method substantially as claimed in Fig. 7 and corresponding text as: forming a semiconductor film (110 and 111) having an amorphous structure over a first substrate (100) [0050]; irradiating the semiconductor film with a laser beam with scanning in a direction, thereby forming a first region and a second region in the semiconductor film [0052]; and forming an integrated circuit comprising a first thin film transistor using the first region in the semiconductor film and a memory cell array comprising a second thin film transistor using the second region in the semiconductor film [0051] (claim 11). Yamazaki teaches the second thin film transistor comprises a gate electrode, a source region and a drain region, and wherein the gate electrode is electrically connected to one of the source region and the drain region [0050-0053] (claim 13). Yamazaki teaches the laser beam is a continuous wave laser beam [0023], and wherein the first region includes a crystal grain grown continuously in the direction of scanning the continuous wave laser beam [0023] (claim 18). Yamazaki teaches an active layer of the first thin film transistor is arranged so that the direction of scanning the laser beam conforms to direction in which an electric carrier moves in the active layer when electric current is flown in the first thin film transistor [0051-0052] (claim 19). Yamazaki teaches the first substrate is selected from

the group consisting of a glass substrate, a quartz substrate, a ceramic substrate and a metal substrate [0050] (claim 21).

Yamazaki lacks anticipation only in not explicitly teaching that: 1) the first region is superior to the second region in crystallinity (claim 11).

Yamazaki teaches that the crystallinity of the TFT regions are different from one another [0023].

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575,1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify; Yamazaki by making the first region is superior to the second region in crystallinity, in order to achieve the optimum level operation.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (U.S. Publication No. 2003/0062845 dated 4/3/2003) as applied to claim 11 above, and further in view of Shimoda et al. (U.S. Publication No. 2003/0022403 dated 1/30/2003).

Yamazaki shows the method substantially as claimed and described in the preceding paragraphs.

Yamazaki lacks anticipation only in not explicitly teaching that: 1) a memory cell; a microprocessor; and at least one of a connection terminal, a rectifier circuit, a demodulator circuit and a modulator circuit (claim 12).

Shimoda discloses a method of forming thin film devices. Shimoda teaches a built-in circuit board is manufactured using the transfer method of the present invention. Specifically, the display panel (171), the fingerprint detector (173), the external terminal (174), the microprocessor (175), the memory (176), the communication circuitry (177) and so on are each made to be chips, and all or some of them are formed in integrated fashion on transfer origin substrates [0383]. This process helps to improve manufacturing efficiency [0045].

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify; Yamazaki by providing a memory cell; a microprocessor; and at least one of a connection terminal, as taught by Shimoda with the motivation of improved efficiency.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (U.S. Publication No. 2003/0062845 dated 4/3/2003) as applied to claim 11 above, and further in view of Kanemori et al. (U.S. Patent No. 6,072,559 dated 6/6/2000).

Yamazaki shows the method substantially as claimed and described in the preceding paragraphs.

Yamazaki lacks anticipation only in not explicitly teaching that: 1) the step of forming an antenna (claim 14).

Kanemori discloses an active matrix display. Kanemori discloses the formation of an antenna formed after the formation of the source/drain electrodes (col. 7, lines 20-40). This helps to reduce the leakage that may occur (col. 3, lines 1-6).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify; Yamazaki by forming an antenna, as taught by Kanemori, with the motivation that it helps to reduce leakage that may occur.

Allowable Subject Matter

9. Claims 15-17, 20 and 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Walter L. Lindsay, Jr./
Primary Examiner, Art Unit 2812

7/16/2009